Amendments to the Claims:

The listing of claims will replace all prior versions, and listings, of claims in the application:

5   **Listing of Claims:**

Claim 1 (Previously Presented): A feed-forward equalizer (FFE) of a communication system comprising:

an adaptive filter for filtering a receiving signal according to a transfer function

10   including a plurality of parameters to eliminate a pre-cursor inter-symbol interference (pre-ISI) of the receiving signal, the adaptive filter comprising:

a plurality of delay elements for generating a plurality of delay signals according to the receiving signal;

a plurality of multiplier for respectively multiplying the receiving signal and the

15   delay signals by the parameters and thereby generating a plurality of multiplied signals, wherein at least one of the parameters remains fixed while the other parameters are adjusted to converged values, so as to accelerate the convergence of the communication system; and

a summing circuit for summing the multiplied signals to generate a filtered

20   receiving signal; and

a digital auto-gain controller (DAGC) coupled to the adaptive filter for adjusting the magnitude of the filtered receiving signal according to the transfer function;

wherein a center multiplier among the multipliers is designated to multiply one of the delay signals by the fixed parameter to generate one of the multiplied signals.

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Claim 2 (Previously Presented): The FFE as claimed in claim 1, wherein at least two of the parameters remain fixed, the center multiplier and an adjacent multiplier neighboring the center multiplier respectively multiply two of the delay signals by

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the two fixed parameters to generate two of the multiplied signals.

Claim 3 (Previously Presented): The FFE as claimed in claim 1, wherein the fixed
parameter utilized by the center multiplier is 1.

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Claim 4 (Previously Presented): The FFE as claimed in claim 1, wherein the transfer
function is $C_0Z^3+C_1Z^2+C_2Z^1+C_3+C_4Z^1+C_5Z^2+C_6Z^3$, wherein C_0, C_1, C_2, C_3, C_4, C_5,
and C_6 are the parameters, Z represents a delay element among the delay elements,
and C_3 is the fixed parameter utilized by the center multiplier.

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Claim 5 (Previously Presented): The FFE as claimed in claim 4, wherein C_3 is 1.

Claim 6 (Currently Amended): The FFE as claimed in claim 4, wherein C_4 is ± 0.5.

15   Claim 7 (Previously Presented): A transceiver of a communication system, comprising:
a front end receiver for receiving a receiving signal and converting the receiving
signal to a first signal with a pre-cursor component and a post-cursor
component;
a noise canceller coupled to the front end receiver for generating a second signal
20   through eliminating the noise of the first signal;
a Feed-Forward Equalizer (FFE) coupled to the noise canceller for generating a third
signal through eliminating the pre-cursor component in the second signal
according to a transfer function including a plurality of parameters, at least one
of the parameters remains fixed while the other parameters are adjusted to
25   converged values, so as to accelerate the convergence of the communication
system, the FFE comprising:
an adaptive filter for filtering a receiving signal according to the transfer function
to eliminate the pre-cursor component, comprising:

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a plurality of delay elements for generating a plurality of delay signals
according to the receiving signal;

a plurality of multiplier for respectively multiplying the receiving signal and
the delay signals by the parameters and thereby generating a plurality of

5   multiplied signals, wherein a center multiplier among the multipliers is
designated to multiply one of the delay signals by the fixed parameter to
generate one of the multiplied signals; and

a summing circuit for summing the multiplied signals to generate a filtered
receiving signal; and

10   a digital auto-gain controller (DAGC) coupled to the adaptive filter for adjusting
the magnitude of the filtered receiving signal according to the transfer
function and thereby generating the third signal; and

a decoding system coupled to the FFE for decoding the third signal and eliminating
the post-cursor component in the third signal.

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Claim 8 (Previously Presented): The transceiver as claimed in claim 7, wherein at least
two of the parameters remain fixed, the center multiplier and an adjacent multiplier
neighboring the center multiplier respectively multiply two of the delay signals by
the two fixed parameters to generate two of the multiplied signals.

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Claim 9 (Previously Presented): The transceiver as claimed in claim 7, wherein the fixed
parameter utilized by the center multiplier is 1.

Claim 10 (Cancelled)

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Claim 11 (Previously Presented): The transceiver as claimed in claim 7, wherein the
transfer function is $C_0Z^3+C_1Z^2+C_2Z^1+C_3+C_4Z^1+C_5Z^2+C_6Z^3$, wherein C_0, C_1, C_2,
C_3, C_4, C_5, and C_6 are the parameters, Z represents a delay element among the delay

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elements, and C_3 is the fixed parameter utilized by the center multiplier.

Claim 12 (Previously Presented): The transceiver as claimed in claim 11, wherein C_3 is 1.

5   Claim 13 (Currently Amended): The transceiver as claimed in claim 12, wherein C_4
is -0.5.

Claim 14 (Currently Amended): A feed-forward equalizer (FFE) of a communication
system comprising:

10   a multi-tap filter for filtering a receiving signal, comprising:

              a plurality of delay elements coupled in series for generating a plurality of delay
              signals according to the receiving signal, each of the delay signals
              corresponding to a different delay, one of the delay signals corresponding to a
              middle delay among the different delays;

15   a plurality of multiplier for respectively multiplying the receiving signal and the
              delay signals by a plurality of parameters and thereby generating a plurality of
              multiplied signals, wherein at least one of the parameters remains fixed while
              the other parameters are adjusted to converged values, so as to accelerate the
              convergence of the communication system; and

20   a summing circuit for summing the multiplied signals to generate a filtered
              receiving signal; and

          a digital auto-gain controller (DAGC) coupled to the adaptive filter for adjusting the
              magnitude of the filtered receiving signal according to the parameters [[.]] ,
              wherein the multipliers are coupled in parallel sequentially and a center multiplier

25   among the multipliers is designated to multiply the delay signal with the middle
              delay by the fixed parameter to generate one of the multiplied signals.

Claim 15 (Previously Presented): The FFE of claim 14, wherein at least two of the

parameters remain fixed while the other parameters are adjusted.

Claim 16 (Previously Presented): The FFE of claim 15, wherein two of the multipliers respectively multiply two of the delay signals by the two fixed parameters.

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Claim 17 (Cancelled)

Claim 18 (Previously Presented): The FFE of claim 16, wherein the two multipliers utilizing the two fixed parameters are coupled adjacently.

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Claim 19 (Cancelled)

Claim 20 (Currently Amended): The FFE of claim [[19]] 14, wherein at least two of the parameters remain fixed, the center multiplier and an adjacent multiplier neighboring the center multiplier respectively are designated to multiply two of the delay signals by the two fixed parameters to generate two of the multiplied signals.

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